TEXAS INSTRUMENTS

SN65LVCP22/23 EVM

User's Guide

June 2003

HPL Interface

SLLU060

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It is important to operate this EVM within the input voltage range between 1.2 V and 3.3 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This user's guide describes the SN65LVCP22/23 evaluation module (EVM). This guide contains the EVM schematic, bill of materials, assembly drawing, and board layouts.

How to Use This Manual

This document contains the following chapters:

- ❏ Chapter 1– Introduction
- ❏ Chapter 2– Setup and Equipment Required
- ❏ Chapter 3– EVM Construction
- ❏ Chapter 4– PCB Fabrication and Bill of Materials

This user's guide may contain cautions and warnings. The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

Related Documentation From Texas Instruments

SN65LVCP22 – LVDS crosspoint switch data sheet (SLLS553)

SN65LVCP23 – LVPECL crosspoint switch data sheet (SLLS554)

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Electrostatic Sensitive Devices



This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

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Chapter 1

Introduction

The SN65LVCP22/23 EVM highlights the high-speed performance and functionality of the SN65LVCP22 and SN65LVCP23 2x2 crosspoint switches.

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1.1 Overview

The SN65LVCP22 (LVDS output) and SN65LVCP23 (LVPECL output) are high-speed 2x2 crosspoint switches. The four different functions that these crosspoints provide are shown in Figure 1–1. The functions of these crosspoints are selected via pins SEL0 and SEL1. Control pins EN0 and EN1 enable or disable the outputs. The receiver has a wide input common-mode voltage range with an ability to accept LVDS, LVPECL and CML signaling levels.

Figure 1–1. Functional Configurations of the SN65LVCP22 and SN65LVCP23

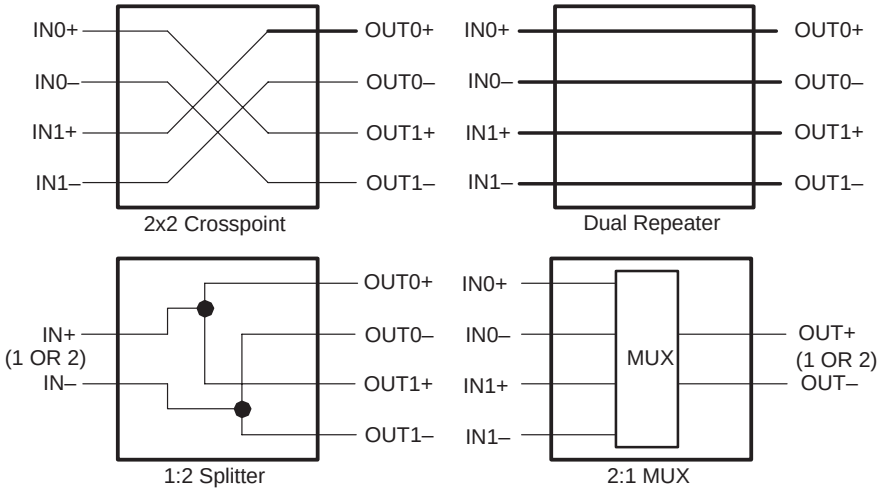
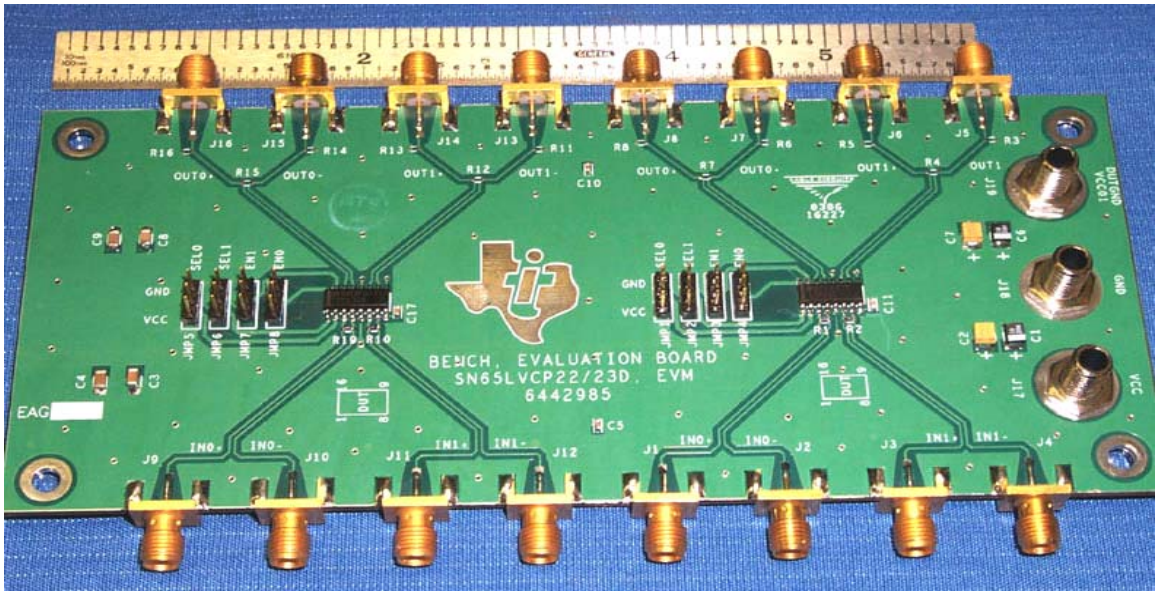


Figure 1–2 is a picture of the SN65LVCP22/23 EVM. The EVM part number is SN65LVCP22/23EVM. The EVM comes with the SN65LVCP22D and SN65LVCP23D (SOIC both) installed. A copy of the datasheet is shipped with the EVM. The latest version of the datasheet is available from www.ti.com.

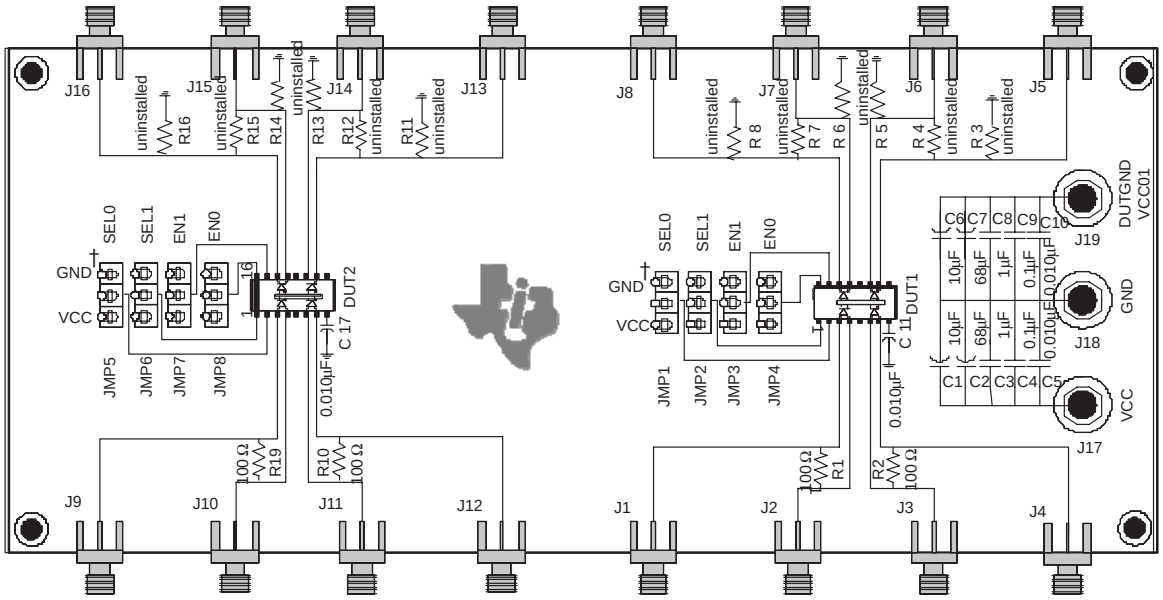
Figure 1–2. SN65LVCP22/23 EVM



1.2 Signal Paths

The signal paths on this EVM include 16 edge-launch SMA connectors (J1–J16) for high-speed data transmission, 4 jumpers (JMP1, JMP2 for DUT1and JMP5, JMP6 for DUT2) for active switch logic control, 4 jumpers (JMP3, JMP4 for DUT1and JMP7, JMP8 for DUT2) for enabling and disabling the outputs, and three banana jacks (J17, J18, J19) for power and ground connections. See Figure 1–3.

Figure 1–3. SN65LVCP22/23 EVM



†GND is tied to Vcc01

Chapter 2

Setup and Equipment Required

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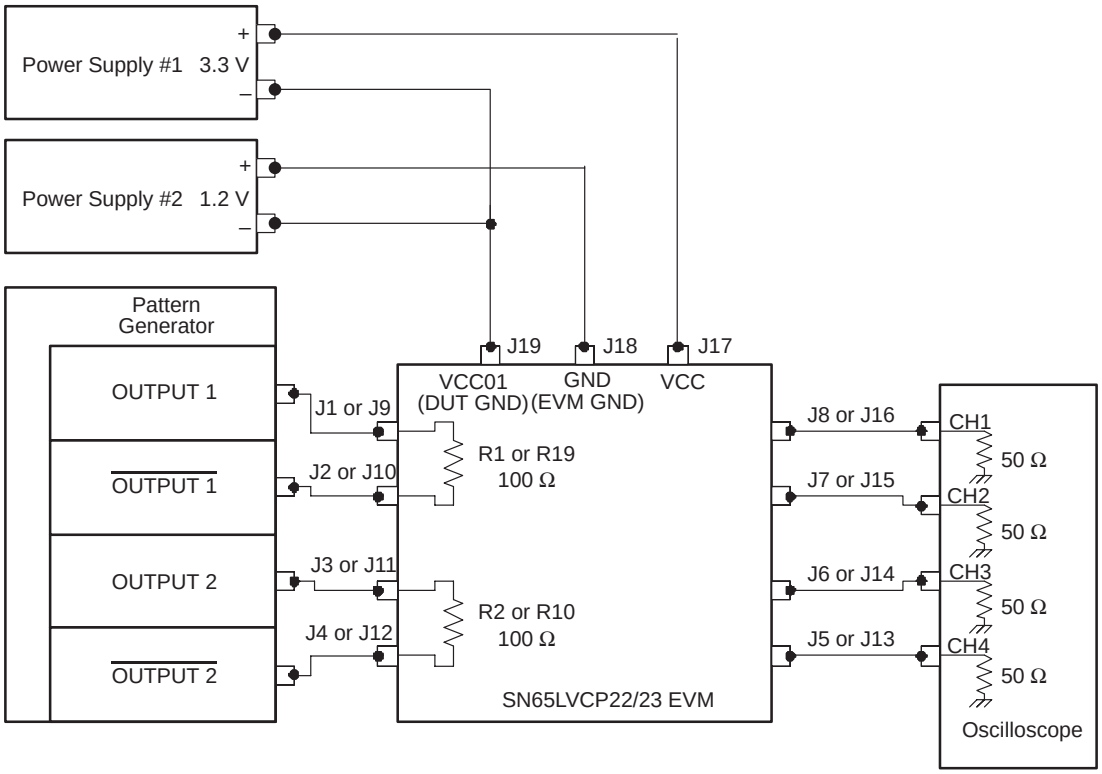
2.1 Overview

The output characteristics of the SN65LVCP23 (LVPECL) drivers are generally loaded with 50-Ω resistors to a termination bias voltage, V_{TT}. V_{TT} is usually 2 V below the supply voltage of the driver circuit. When the driver operates from a 3.3-V supply, V_{TT} is set to approximately 1.3 V.

The output characteristics of the SN65LVCP22 are specified in the TIA/EIA-644 standard. LVDS drivers nominally provide a 350-mV differential signal, with a 1.25–V offset from ground. These levels are attained when driving a 100-Ω differential line-termination test load. This requirement includes the effects of up to 32 standard receivers with their ground reference up to 1 V different from that of the driver. This common-mode loading limitation of LVDS drivers affects how they are observed and much of the test setup that follows..

The EVM is designed to support the SN65LVCP22 LVDS output device as well as the SN65LVCP23 LVPECL output device. By using the three power jacks (J17, J18, J19), as well as installing termination resistors (R3–R8 and R11–R16), different methods of termination and probing can be used to evaluate the device output characteristics. The typical setup for the SN65LVCP22 is shown in Figure 2–1.

Figure 2–1. EVM Power Connections for SN65LVCP22/23 Evaluation—With LVDS Inputs

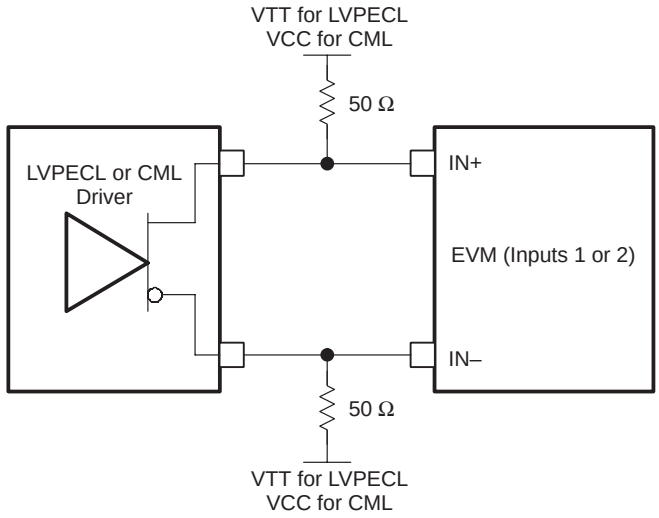


2.2 Applying an Input

When using a general-purpose signal generator with 50-Ω output impedance, make sure that the signal levels are between 0-V and 4-V with respect to J19, device under test ground (DUT GND), designated as Vcc01.

Inputs should be applied to the SMA connectors J1, J2, J3, and J4 for DUT1 (or J9, J10, J11 and J12 for DUT2). Matched cable lengths must be used when connecting the signal generator to the EVM to avoid inducing skew between the noninverting and inverting inputs. The EVM comes with 100-Ω resistors installed across the differential inputs for LVDS termination. The simple 100-Ω terminations do not provide the necessary termination for LVPECL or CML[1] output structures. In order to interface the SN65LVCP22/23 EVM with CML or LVPECL drivers, external terminations are required. Figure 2–2 shows an example termination for LVPECL and CML output structures. Remove resistors R1, R2, R10 and R19 when using the external terminations.

Figure 2–2. External Termination for Interfacing CML or LVPECL Drivers



The use of external resistors creates a significant stub between the termination and the actual device receivers. The user needs to verify that the transition time of the input signal, coupled with the stub length, does not lead to reflection problems. In normal applications, the termination would be placed as close as possible to the device inputs to minimize reflections.

The control lines SEL0 and SEL1 require LVTTL levels and are stimulated by the Vcc power supply, via jumpers JMP1 and JMP2 (DUT1) and JMP5 and JMP6 (DUT2). Table 2–1 shows the different functions and the control line settings for each.

[1]CML is not a standardized physical layer and therefore the output structures and required termination differ from vendor to vendor.

Table 2–1. Crosspoint Function Table

SEL0	SEL1	OUT0	OUT1	Function
0	0	IN0	IN0	1:2 Splitter
0	1	IN0	IN1	Repeater
1	0	IN1	IN0	Switch
1	1	IN1	IN1	1:2 Splitter

2.3 Observing an Output

Direct connection to an oscilloscope with 50–Ω internal terminations to ground is accomplished without R3–R8 (DUT1) and R11–R16 (DUT2) installed. The outputs are available at J5–J8 (DUT1) and J13–J16 (DUT2) for direct connection to oscilloscope inputs. Matched cable lengths must be used when connecting the EVM to a scope to avoid inducing skew between the noninverting (+) and inverting (–) outputs.

The three power jacks (J17, J18, J19) are used to provide power and a ground reference for the EVM. The power connections to the EVM determine the common-mode load to the device. As mentioned earlier, LVDS drivers have limited common-mode driver capability. When connecting the EVM outputs directly to oscilloscope inputs, setting of the oscilloscope common-mode offset voltage is required, as the oscilloscope presents low common-mode load impedance to the device.

Returning to Figure 2–1, power supply 1 is used to provide the required 3.3 V to the EVM. Power supply 2 is used to offset the EVM ground relative to the DUT ground. The EVM ground is connected to the oscilloscope ground through the returns on SMA connectors J5–J8 (DUT1) and J13–J16 (DUT2). With power applied as shown in Figure 2–1, the common-mode voltage seen by the SN65LVCP22 is approximately equal to the reference voltage being used inside the device, preventing significant common-mode current to flow. Optimum device setup can be confirmed by adjusting the voltage on power supply 2 until its current is minimized. It is important to note that use of the dual supplies and offsetting the EVM ground relative to the DUT ground are simply steps needed for the test and evaluation of devices. Actual designs include high-impedance receivers, which do not require the setup steps outlined above.

LVPECL drivers need a 50-Ω termination to V_{TT}. A modification of Figure 2–1 and the above instructions are used when evaluating an SN65LVCP23 with a direct connection to a 50-Ω oscilloscope. With power supply 1 in Figure 2–1 set to 3.3 V, power supply 2 should be set to 1.3 V (2 V below Vcc) to provide the correct termination voltage.

If the outputs are to be evaluated with a high-impedance probe, direct probing on the EVM board is supported via installation of a 50-Ω resistor across the solder pads for R6 and R8, and another 50-Ω resistor across the solder pads for R3 and R5 for DUT1. Or, LVDS outputs can be observed by installing a 100-Ω resistor at R4, R7, R12, or R15. LVPECL outputs can be observed by installing R3, R5, R11, R13, R14, and R16 (49.9-Ω resistors) and setting power supply #2 to 1.3 V. (Note that power supply #2 must be able to sink current.)

2.4 Typical Test Results

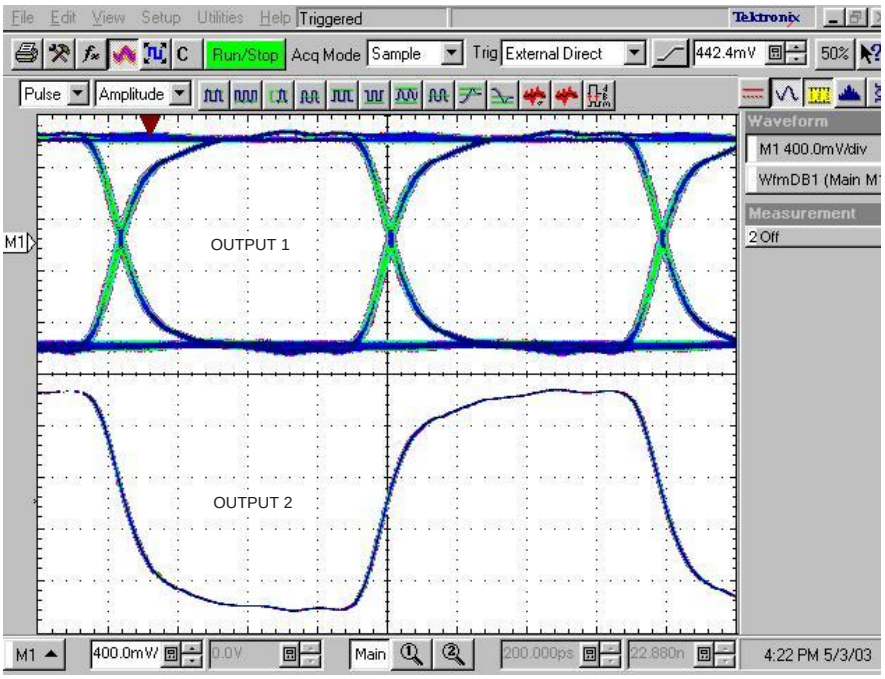
Figure 2–3 is a typical result obtained with the EVM setup shown in Figure 2–1. The upper waveform is the difference voltage between channels 1 and 2 of the oscilloscope and the lower trace is the difference voltage between channels 3 and 4. The DUT was configured to send the IN0+/IN0– inputs to the outputs OUT0+/OUT0– and inputs IN1+/IN1– to outputs OUT1+/OUT1– by setting EN0 and EN1 to a high level and by setting SEL0 to Gnd and SEL1 to Vcc. The stimuli were a 2^{23}–1 PRBS to J1 and J2 at 1.3 Gbps, and a 650 MHz clock to J3 and J4. The input levels for both clock and data were a differential voltage of 400 mV, with a common-mode voltage of 0 V (referenced to the ground of the pattern generator).

Figure 2–3. Typical Test Results of the SN65LVCP23 with the SN65LVCP22/23EVM

1.3 Gbps
2^{23} –1 PRBS

V_{CC} = 3.3 V
$|V_{ID}|$ = 200 mV, V_{IC} = 1.2 V
Vertical Scale=400mV/div

650 MHz



Horizontal Scale = 200 ps

Chapter 3

EVM Construction

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3.1 Schematics

Figure 3–1. SN65LVCP22D Schematic

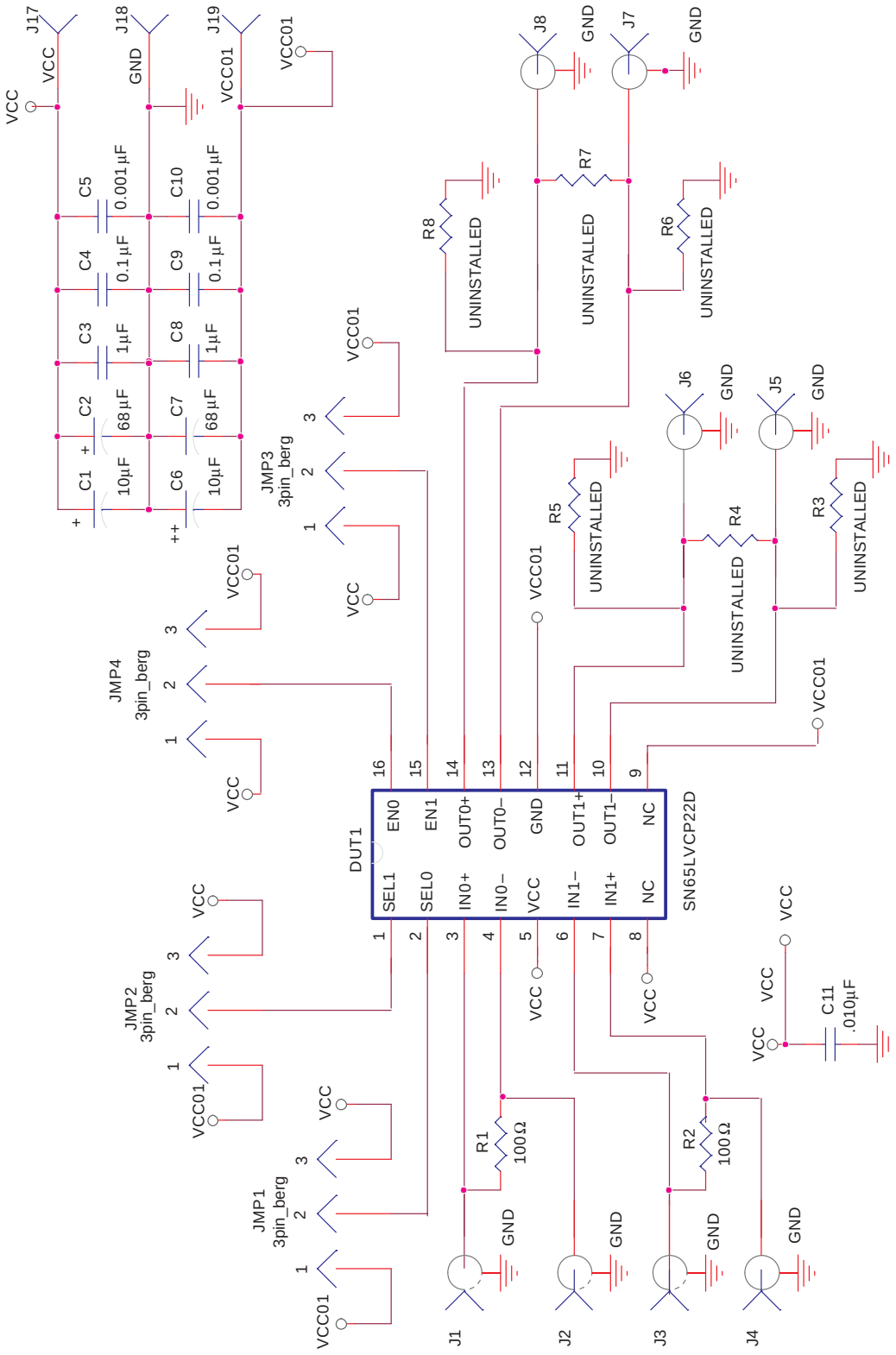
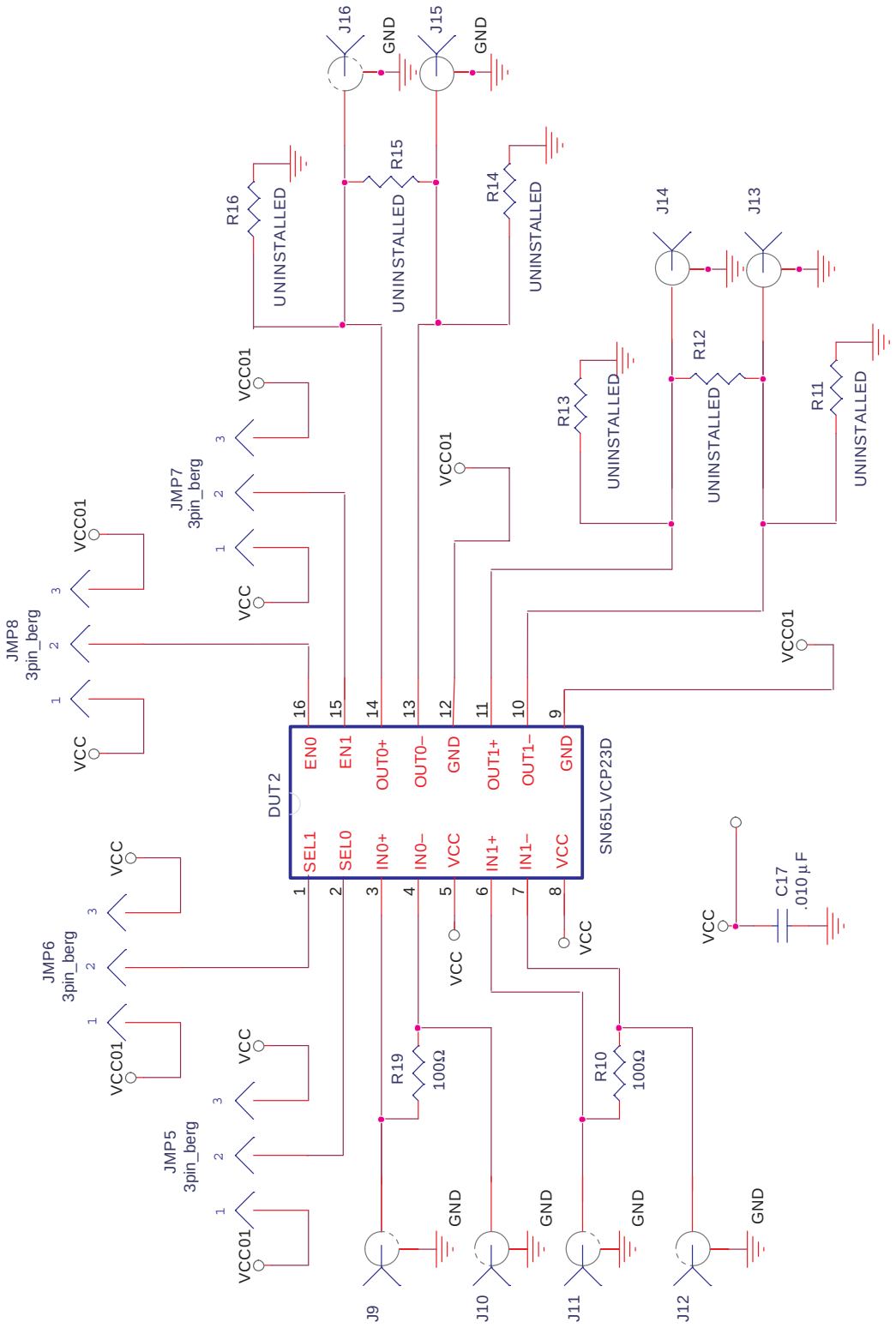


Figure 3–2. SN65LVCP23D Schematic



3.2 Board Layout Patterns

Figure 3–3. SN65LVCP22/23 Silk Screen

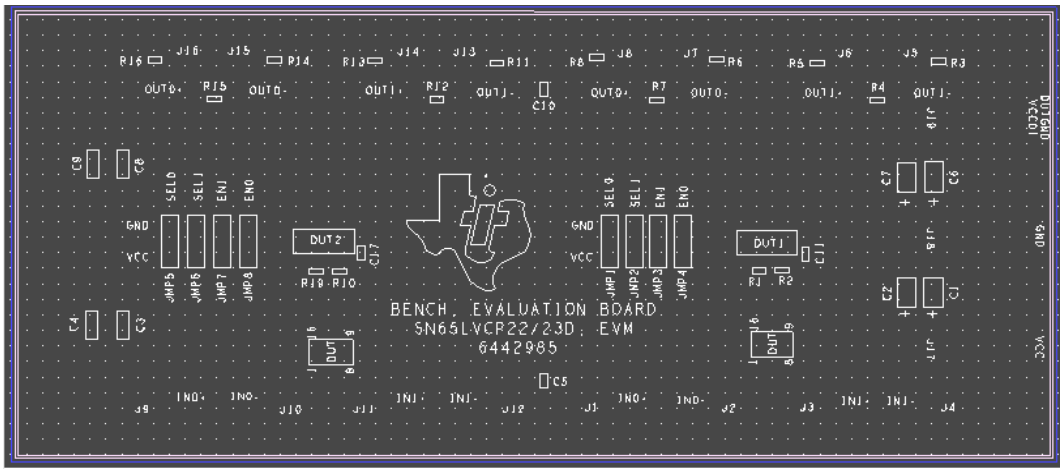


Figure 3–4. Layer 1 – Signal Plane

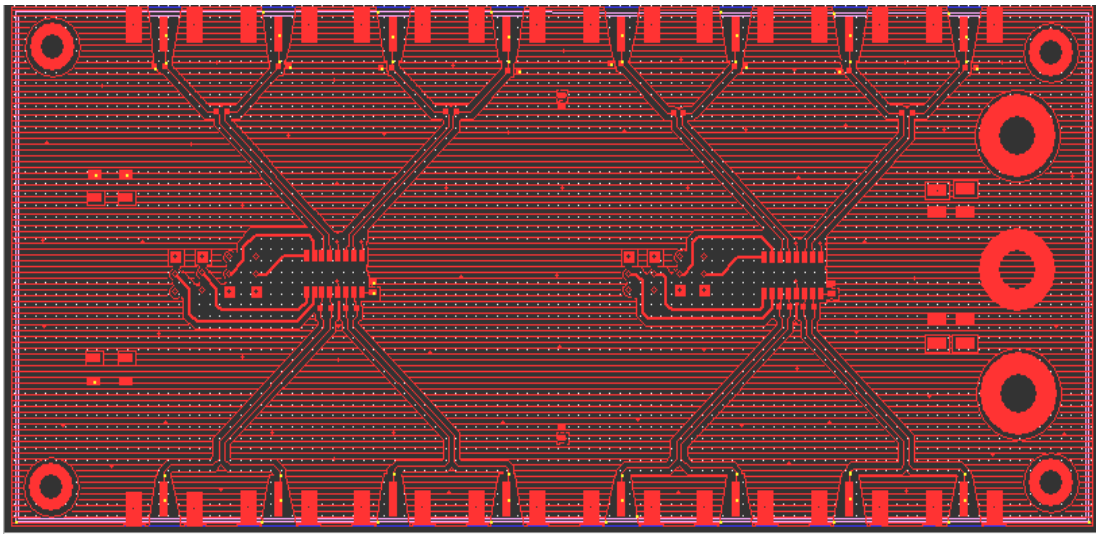


Figure 3–5. Layer 2 – GND Plane

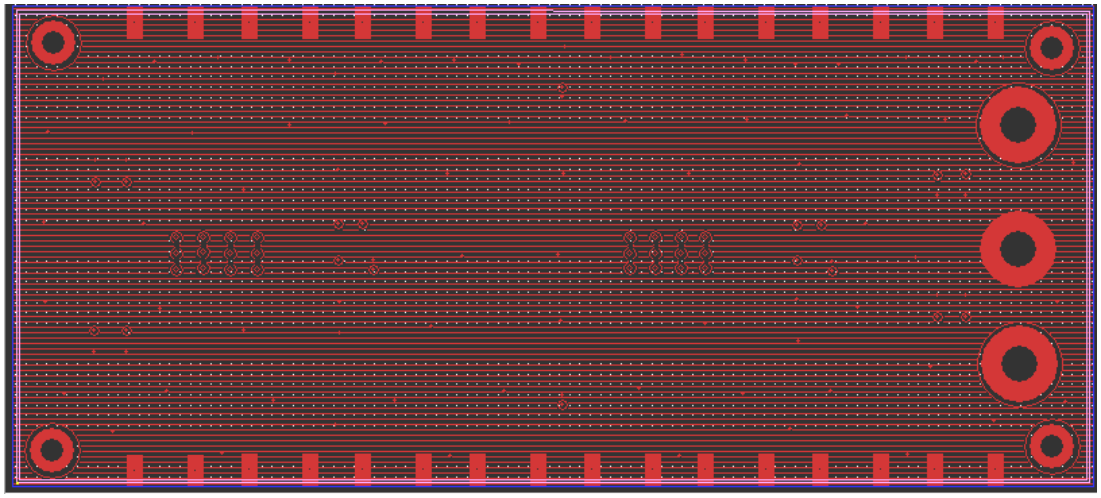


Figure 3–6. Layer 3 – Split Plane (V_{CC}/V_{CC01})

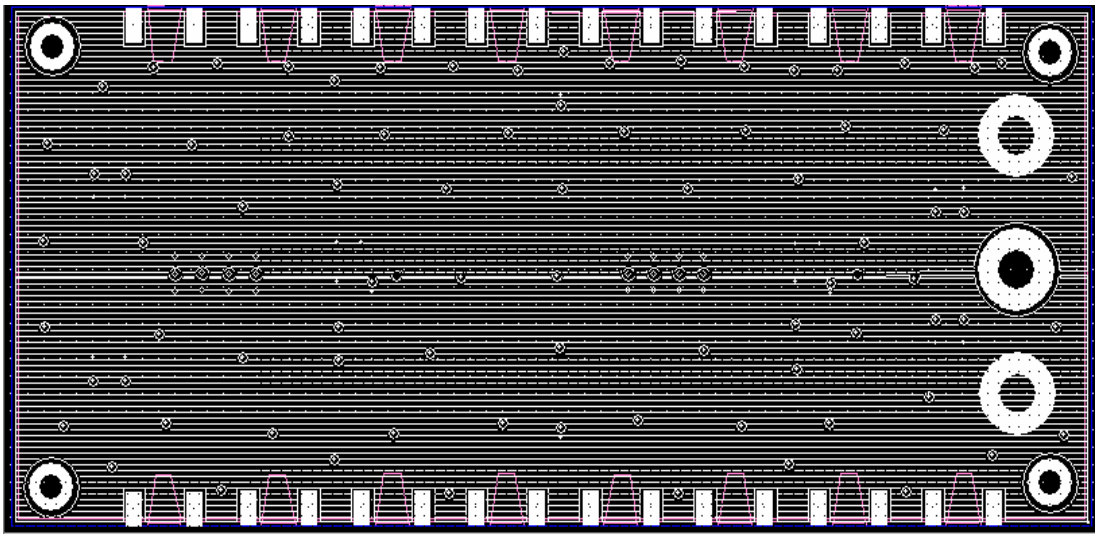
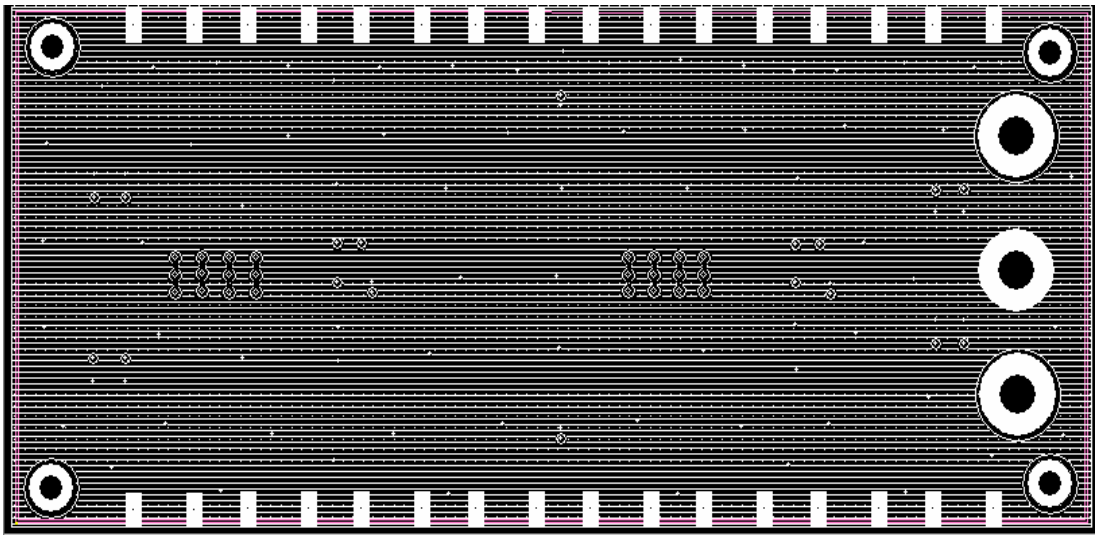


Figure 3–7. Layer 4 – GND Plane



Chapter 4

PCB Fabrication and Bill of Materials

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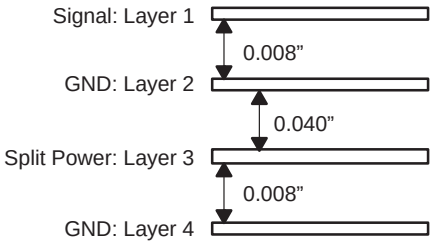
4.2 Bill of Materials 4-2

4.1 PCB Fabrication Notes and Stackup

Notes:

1) All fabrication items must meet or exceed best industry practice. IPC–A 600C (Commercial Std.)
2) Laminate material NELCO N4000–13 [DO NOT USE–13SI]
3) Copper weight: 1 oz start internal and 1/2 oz start external
4) Finished board thickness: 0.62” ±0.10”
5) Maximum warp and twist to be 0.005 inch per inch
6) Minimim copper wall thickness of plate-through holes 0.002 inch
7) Minimum annular ring of plate-through holes to be 0.001 inch
8) Minimum allowable line reduction to be 20% or 0.002 inch whichever is greater
9) 0.0125 inch signal lines on layer 1 to be impednace controlled 100 Ω to each other ±10%
10) Dielectric constants are core 3.9
11) Fill vias that are in a pad are prepreg 3.9

Stackup



4.2 Bill of Materials for SN65LVCP22/23 EVM

Comment	Quantity	Components
10 µF, 35V, 10%	2	C1, C6
68 µF, 10 V, 20%, Low ESR	2	C2, C7
1 µF, 25 V +80% –20%	2	C3, C8
0.1 µF, 50 V, 5%	2	C4, C9
0.001 µF, 25 V, 5%	2	C5, C10
0.01 µF, 50 V, ±10%	2	C11, C17
SN65LVCP22D	1	DUT1
SN65LVCP23D	1	DUT2
3POS_JUMPER	8	JMP1, JMP2, JMP3, JMP4, JMP5, JMP6, JM7, JMP8
SMA_PCB_MT_MOD	16	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16
Banana Jack	3	J17, J18, J19
100 Ω, 1/4 Watt, 1%	4	R1, R2,R10,R19
49.9 Ω, 1/4 Watt, 1% (uninstalled)	12	R3, R4, R5, R6, R7, R8, R11, R12, R13, R14, R15, R16